WHAT IS CLAIMED IS:

1. A signal line drive circuit, including:

a high-voltage side switch block and a low-voltage side switch block;

a ladder resistor across which a high-voltage side voltage and a low-voltage side voltage are applied through a high-voltage side selection switch selected from said high-voltage side switch block and a low-voltage side selection switch selected from said low-voltage side switch block, respectively; and

a plurality of intermediate voltage takeout signal lines which take out a first intermediate voltage from an end point, connected to the high-voltage side selection switch, of said ladder resistor and which then take out a second and a third, ... and $(k-1)$th intermediate voltage from any other end points thereof in the order of closeness to the high-voltage side selection switch and which take out a kth intermediate voltage from an end point, connected to the low-voltage side selection switch, of said ladder resistor, where k is an integer greater than or equal to 2,

wherein a dividing resistance value which causes a difference between the first intermediate voltage and the second intermediate voltage among resistance components in said ladder resistor is greater than an on-resistance value of the high-voltage side selection switch.

2. A signal line drive circuit, including:

a high-voltage side switch block and a low-voltage side switch block;

a ladder resistor across which a high-voltage side voltage and a low-voltage side voltage are applied through a high-voltage side selection switch selected from said high-voltage side switch block and a low-voltage side selection switch selected from said low-voltage side switch block, respectively; and

a plurality of intermediate voltage takeout signal lines which take out a first intermediate voltage from an end point, connected to the high-voltage side selection switch, of said ladder resistor and which then take out a second and a third, ... and $(k-1)$th intermediate voltage from any other end points thereof in the order of closeness to the high-voltage side selection switch and which take out a kth intermediate voltage from an end point, connected to the low-voltage side selection switch, of said ladder resistor, where k is an integer greater than or equal to 2,

wherein a dividing resistance value which causes a difference between the $(k-1)$th intermediate voltage and the kth intermediate voltage among resistance components in said ladder resistor is greater than an on-resistance value of the high-voltage side selection switch.

3. A signal line drive circuit, including:

a high-voltage side switch block and a low-voltage side switch block;

a ladder resistor across which a high-voltage side voltage and a low-voltage side voltage are applied through a high-voltage side selection switch selected from said high-voltage side switch block and a low-voltage side selection switch selected from said low-voltage side switch block, respectively; and

a plurality of intermediate voltage takeout signal lines which take out different intermediate voltages, respectively, from any end points of said ladder resistor,

wherein the signal line drive circuit is structured such that a relationship of a potential difference between the high-voltage side voltage and a predetermined reference voltage and that between the low-voltage side voltage and the reference voltage and a relationship of on-resistance values of said high-voltage side and low-voltage side switches are reversed.

4. A signal line drive circuit according to Claim 1, including:

an upper selection circuit which receives an input of x bits out of n-bit image signals and selects the high-voltage side selection switch and the low-voltage side selection switch from said high-voltage side switch block

and said low-voltage side switch block, respectively, where n is an integer greater than or equal to 2 and x is an integer greater than or equal to 1 and less than n; and

a lower selection circuit which selects a desired intermediate voltage takeout signal line from said plurality of intermediate voltage takeout signal lines by signals of (n-x) bits, excluding the x bits, among the image signals.

5. A signal line drive circuit according to Claim 2, including:

an upper selection circuit which receives an input of x bits out of n-bit image signals and selects the high-voltage side selection switch and the low-voltage side selection switch from said high-voltage side switch block and said low-voltage side switch block, respectively, where n is an integer greater than or equal to 2 and x is an integer greater than or equal to 1 and less than n; and

a lower selection circuit which selects a desired intermediate voltage takeout signal line from said plurality of intermediate voltage takeout signal lines by signals of (n-x) bits, excluding the x bits, among the image signals.

6. A signal line drive circuit according to Claim 3, including:

an upper selection circuit which receives an input of x bits out of n-bit image signals and selects the high-

voltage side selection switch and the low-voltage side selection switch from said high-voltage side switch block and said low-voltage side switch block, respectively, where n is an integer greater than or equal to 2 and x is an integer greater than or equal to 1 and less than n; and

a lower selection circuit which selects a desired intermediate voltage takeout signal line from said plurality of intermediate voltage takeout signal lines by signals of (n-x) bits, excluding the x bits, among the image signals.

7. A signal line drive circuit according to Claim 4, wherein said upper selection circuit is such that logic to select the high-voltage side selection switch and the low-voltage selection switch exists outside the path of lines on which a plurality of switches included in said switch blocks is interposed, and wherein said lower selection circuit is such that at least part of logic to select a desired one of said plurality of intermediate voltage takeout signal lines is interposed on the path of said plurality of intermediate voltage takeout signal lines.

8. A signal line drive circuit according to Claim 5, wherein said upper selection circuit is such that logic to select the high-voltage side selection switch and the low-voltage selection switch exists outside the path of lines on which a plurality of switches included in said switch blocks are

interposed, and wherein said lower selection circuit is such that at least part of logic to select a desired one of said plurality of intermediate voltage takeout signal lines is interposed on the path of said plurality of intermediate voltage takeout signal lines.

9. A signal line drive circuit according to Claim 6, wherein said upper selection circuit is such that logic to select the high-voltage side selection switch and the low-voltage selection switch exists outside the path of lines on which a plurality of switches included in said switch blocks are interposed, and wherein said lower selection circuit is such that at least part of logic to select a desired one of said plurality of intermediate voltage takeout signal lines is interposed on the path of said plurality of intermediate voltage takeout signal lines.